Tutorial 4 November 2014 **Course: Logical Organization of Computers**

PID:_____ Name: _____ Marks: _____/30

1. Design a logic circuit that
   a. considers a six bit words and passes if a positive signal is given
   b. inverts a six bits word from an input register into an output register.
   c. acts as a controlled inverter.
2. Draw 1 to 10 decoder using AND gates.
3. Complete following truth table. From the truth table find out equation. Also draw equivalent logic circuit for the same.

A	B	C	X= ABC	Y= AB'C'	Z= A'B'C	L= A'BC'	X+Y+Z+L
0	0	0	0	0	0	0	0
0	**0**	**1**	0	0	1	0	1
0	**1**	**0**	0	0	0	1	1
0	1	1	0	0	0	0	0
1	**0**	**0**	0	1	0	0	1
1	0	1	0	0	0	0	0
1	1	0	0	0	0	0	0
1	**1**	**1**	1	0	0	0	1

4. Consider the truth table find out equation represented by X. Also draw equivalent logic circuit for the same.

A	**B**	**C**	**X**
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

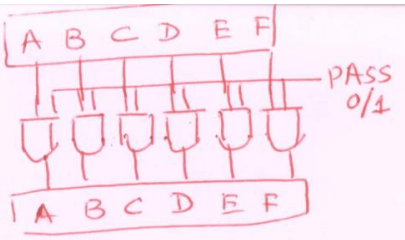
5. Draw logic circuit of 2's complement adder subtractor. Also state objective of this circuit diagram.
6. Define latch. Give circuit diagram of a SR latch with truth table.
7. Draw circuit diagram of a buffer register. Define how may flip-flops are needed to construct a register capable of storing a byte?
8. What is a counter? Draw circuit of a ring counter.

------xxx---xx---xxx-----

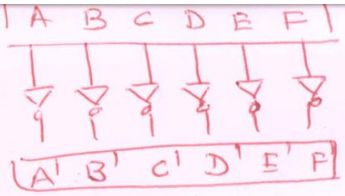
Please verify the solution….

1.

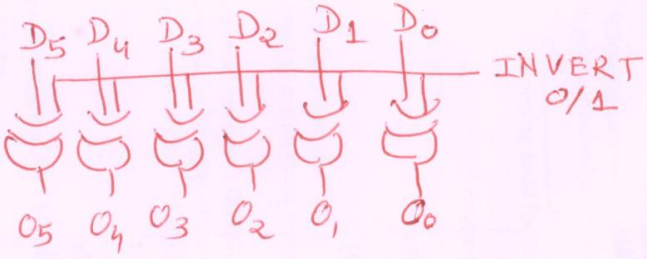
(a)



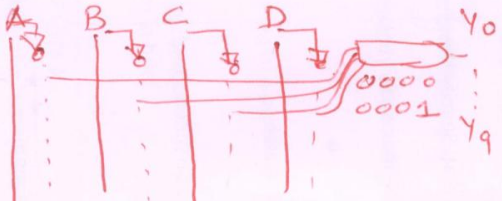
(b)



(c)



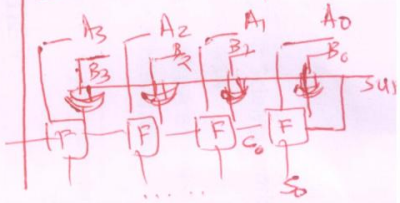
2.



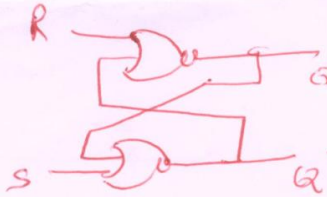
3

It is an XOR gate TT for 3 inputs A, B & C.

5. 2's comp. A/S



6 R



R	S	Q	Comments
0	0	NC	No change
0	1	1	Set
1	0	0	Reset
1	1	*	Race.

It is a device with 2 stable states, it remains in a state till it is triggred to the other.

4. Eq = $A'B'C + AB'C + A$

$= (A' + A)B'C + ABC$

$= B'C + ABC$

7. Buffer Register : X_3 X_2 X_1 X_0

For Byte, 8 bits are there, B.F. requires 8 registers.

8. Ring Counter :